WHAT IS CLAIMED IS:

1. An apparatus comprising:

an instruction decoder;

at least one control register coupled to the instruction decoder; and

an add-compare-select (ACS) engine coupled to the at least one control register;

wherein the instruction decoder is operative to control the ACS engine to perform Viterbi decoding in response to the instruction decoder receiving a first instruction, and the instruction decoder is further operative to control the ACS engine to perform turbo decoding in response to the instruction decoder receiving a second instruction.

2. The apparatus of claim 1, wherein the ACS engine includes:

a plurality of ACS units to perform ACS operations;

a branch metric register coupled to the ACS units to supply branch metric data to the ACS units; and

a plurality of accumulators coupled to the ACS units to store results of the ACS operations performed by the ACS units.

3. The apparatus of claim 2, further comprising:

a memory coupled to the ACS units, to the branch metric register, and to the accumulators.

4. The apparatus of claim 3, wherein in a first mode of operating the apparatus at least some operands are supplied to the ACS units from the accumulators and in a second mode of operating the apparatus at least some operands are supplied to the ACS units from the memory.

5. The apparatus of claim 2, wherein the plurality of accumulators includes four accumulators.

6. The apparatus of claim 5, wherein each of the accumulators includes eight units, each unit being capable of storing 48 bits.

7. The apparatus of claim 6, wherein the 48 bits stored in each accumulator unit include 16 guard bits.

8. The apparatus of claim 2, wherein each of the ACS units is capable of performing butterfly operations.

9. The apparatus of claim 8, wherein:

a final add of a butterfly operation performed by one of the ACS units is a two-operand add if the ACS engine is performing Viterbi decoding; and

the final add of the butterfly operation is a three-operand add if (a) the ACS engine is performing turbo decoding and (b) a certain intermediate result is obtained during the final add.

10. The apparatus of claim 9, wherein an operand for the three-operand add is looked up in a look up table if (a) the ACS engine is performing turbo decoding and (b) the certain intermediate result is obtained during the final add.

11. A system comprising:

a forward error correction decoder; and

a speaker coupled to the forward error correction decoder to audibly reproduce corrected data output from the forward error correction decoder;

wherein the forward error correction decoder includes:

an instruction decoder;

at least one control register coupled to the instruction decoder; and

an add-compare-select (ACS) engine coupled to the at least one control register;

wherein the instruction decoder is operative to control the ACS engine to perform Viterbi decoding in response to the instruction decoder receiving a first instruction, and the instruction decoder is further operative to control the ACS engine to perform turbo decoding in response to the instruction decoder receiving a second instruction.

12. The system of claim 11, wherein the ACS engine includes:

a plurality of ACS units to perform ACS operations;

a branch metric register coupled to the ACS units to supply branch metric data to the ACS units; and

a plurality of accumulators coupled to the ACS units to store results of the ACS operations performed by the ACS units.

13. The system of claim 12, wherein the forward error correction decoder further includes:

a memory coupled to the ACS units, to the branch metric register, and to the accumulators.

14. The system of claim 13, wherein in a first mode of operating the system at least some operands are supplied to the ACS units from the accumulators and in a second mode of operating the system at least some operands are supplied to the ACS units from the memory.

15. The system of claim 12, wherein the plurality of accumulators includes four accumulators.

16. The system of claim 15, wherein each of the accumulators includes eight units, each unit being capable of storing 48 bits.

17. The system of claim 16, wherein the 48 bits stored in each accumulator unit include 16 guard bits.

18. The system of claim 12, wherein each of the ACS units is capable of performing butterfly operations.

19. The system of claim 18, wherein:

a final add of a butterfly operation performed by one of the ACS units is a two-operand add if the ACS engine is performing Viterbi decoding; and

the final add of the butterfly operation is a three-operand add if (a) the ACS engine is performing turbo decoding and (b) a certain intermediate result is obtained during the final add.

20. The system of claim 19, wherein an operand for the three-operand add is looked up in a look up table if (a) the ACS engine is performing turbo decoding and (b) the certain intermediate result is obtained during the final add.

21. A method comprising:

providing a forward error correction decoder which includes an instruction decoder;

operating the forward error correction decoder to perform Viterbi decoding if the instruction decoder receives a first instruction; and

operating the forward error correction decoder to perform turbo decoding if the instruction decoder receives a second instruction.

22. The method of claim 21, wherein the first instruction is provided to the instruction decoder if voice data is to be decoded by the forward error correction decoder.

23. The method of claim 21, wherein the second instruction is provided to the instruction decoder if image data is to be decoded by the forward error correction decoder.